

Dual Matched Low Noise Precision Op Amp and Dual High Speed Low Noise Precision Op Amp

FEATURES

- Guaranteed $80\mu\text{V}$ Max. V_{OS}
- Guaranteed $6.0\text{nV}/\sqrt{\text{Hz}}$ 10Hz Voltage Noise Density
- Guaranteed $3.9\text{nV}/\sqrt{\text{Hz}}$ 1kHz Voltage Noise Density
- Guaranteed $1\mu\text{V}/^\circ\text{C}$ Max. V_{OS} Drift
- Guaranteed 1 Million Min. Voltage Gain
- Guaranteed Matching Characteristics
- Guaranteed $10\text{V}/\mu\text{s}$ Min. Slew Rate (OP-237)

APPLICATIONS

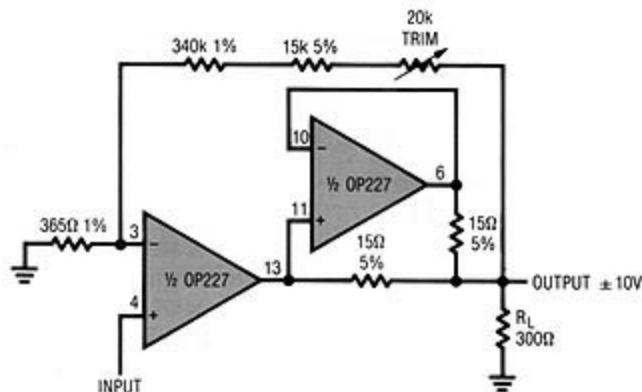
- Instrumentation Amplifiers
- Low Level Signal Processing
- Low Noise Audio Amplifiers
- Strain Gauge Amplifiers

DESCRIPTION

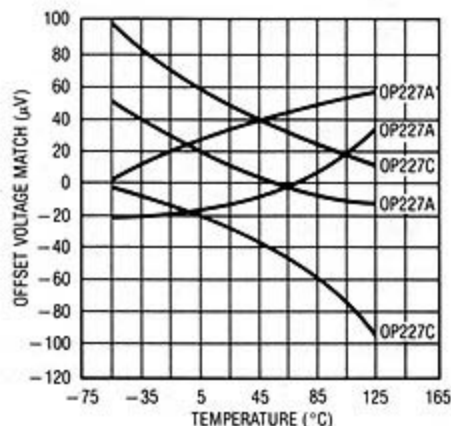
The OP-227 is a dual matched precision op amp which combines low offset, low noise, and high gain with excellent matching characteristics. Typical individual amplifier specifications of $20\mu\text{V}$ V_{OS} , $0.2\mu\text{V}/^\circ\text{C}$ drift, 10nA I_B and $2.8\text{nV}/\sqrt{\text{Hz}}$ 10Hz noise voltage density make the OP-227 an impressive performer in terms of single amplifiers. Matching characteristics are specified with guaranteed limits on all critical parameters including V_{OS} , V_{OS} drift, I_{BIAS} and CMRR (see the Features section), which make the OP-227 an ideal choice for two and three op amp instrumentation amplifier applications.

The OP-237 offers DC specifications identical to the OP-227 and is decompensated for higher speed operation at inverting gains greater than 5.

**Precision Amplifier Drives 300Ω Load to $\pm 10\text{V}$
with 0.05% Accuracy**



**Matching Characteristic;
Drift of Offset Voltage Match
of Representative Units**

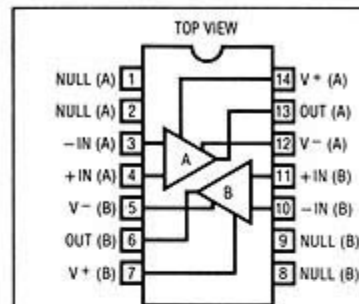


OP-227/OP-237

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 9)	± 22V
Internal Power Dissipation	500mW
Input Voltage	Equal to Supply Voltage
Output Short-Circuit Duration	Indefinite
Differential Input Current (Note 8)	± 25mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature	
OP-227A/237A/227C/237C	-55°C to +125°C
OP-227E/237E/227G/237G	-25°C to +85°C
Lead Temperature Range (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



J PACKAGE 14 PIN HERMETIC
N PACKAGE 14 PIN PLASTIC

NOTE: DEVICE MAY BE OPERATED EVEN IF INSERTION IS REVERSED; THIS IS DUE TO INHERENT SYMMETRY OF PIN LOCATIONS OF AMPLIFIERS A AND B (NOTE 9).

ORDER PART NUMBER
OP-227AJ OP-237AJ
OP-227CJ OP-237CJ
OP-227EJ OP-237EJ
OP-227GJ OP-237GJ
OP-227EN OP-237EN
OP-227GN OP-237GN

ELECTRICAL CHARACTERISTICS Individual Amplifiers

V_S = ± 15V, T_A = 25°C, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	OP-227A, E OP-237A, E			OP-227C, G OP-237C, G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OS}	Input Offset Voltage	(Note 1)	—	20	80	—	60	180	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term V _{OS} Stability	(Notes 2, 3)	—	0.2	1.0	—	0.2	2.0	μV/Mo
I _{OS}	Input Offset Current		—	7	35	—	12	75	nA
I _B	Input Bias Current		—	± 10	± 40	—	± 15	± 80	nA
e _{np-p}	Input Noise Voltage	0.1Hz to 10Hz (Notes 3, 5)	—	0.06	0.20	—	0.06	0.28	μVp-p
e _n	Input Noise Voltage Density	f ₀ = 10Hz (Note 3)	—	2.8	6.0	—	2.8	9.0	nV/√Hz
		f ₀ = 30Hz (Note 3)	—	2.6	4.7	—	2.6	5.9	nV/√Hz
		f ₀ = 1000Hz (Note 3)	—	2.5	3.9	—	2.5	4.6	nV/√Hz
i _n	Input Noise Current Density	f ₀ = 10Hz (Notes 3, 6)	—	1.5	4.5	—	1.5	—	pA/√Hz
		f ₀ = 30Hz (Notes 3, 6)	—	1.0	2.5	—	1.0	—	pA/√Hz
		f ₀ = 1000Hz (Notes 3, 6)	—	0.4	0.7	—	0.4	0.7	pA/√Hz
	Input Resistance—Common Mode		—	7	—	—	5	—	GΩ
	Input Voltage Range		± 11.0	± 12.5	—	± 11.0	± 12.5	—	V
CMRR	Common Mode Rejection Ratio	V _{CM} = ± 11V	114	126	—	100	126	—	dB
PSRR	Power Supply Rejection Ratio	V _S = ± 4V to ± 18V	—	1	10	—	2	20	μV/V
A _{VOL}	Large-Signal Voltage Gain	R _L ≥ 2kΩ, V ₀ = ± 12V	3	20	—	2	20	—	V/μV
		R _L ≥ 600Ω, V ₀ = ± 10V	1	12	—	0.8	12	—	V/μV
V _{OUT}	Output Voltage Swing	R _L ≥ 2kΩ	± 12.0	± 13.8	—	± 11.5	± 13.5	—	V
		R _L ≥ 600Ω	± 10.0	± 12.5	—	± 10.0	± 12.5	—	V
SR	Slew Rate	OP-227 R _L ≥ 2kΩ	1.7	2.8	—	1.7	2.8	—	V/μs
		OP-237 A _{VCL} ≥ 5	10	15	—	10	15	—	V/μs
GBW	Gain Bandwidth Prod.	OP-227 f ₀ = 100kHz (Note 4)	5	8	—	5	8	—	MHz
		OP-237 f ₀ = 10kHz (Note 4)	35	63	—	35	63	—	MHz
		OP-237 f ₀ = 1MHz (A _{VCL} ≥ 5)	—	40	—	—	40	—	MHz
Z ₀	Open-Loop Output Resistance	V ₀ = 0, I ₀ = 0	—	70	—	—	70	—	Ω
P _d	Power Consumption	Each Amplifier	—	80	140	—	90	170	mW
	Offset Adjustment Range	R _p = 10kΩ	—	± 4	—	—	± 4	—	mV

ELECTRICAL CHARACTERISTICS Individual Amplifiers $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		OP-227E OP-237E			OP-227G OP-237G			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●	—	40	140	—	85	280	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●	—	0.2	1.0	—	0.3	1.8	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	—	15	50	—	20	135	nA
I_B	Input Bias Current		●	—	± 20	± 60	—	± 35	± 150	nA
	Input Voltage Range		●	± 10.5	± 11.5	—	± 10.5	± 11.5	—	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	110	124	—	96	118	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	—	2	15	—	2	32	$\mu V/V$
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	1	14	—	0.8	14	—	$V/\mu V$
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 11.7	± 13.6	—	± 11.0	± 13.3	—	V

ELECTRICAL CHARACTERISTICS Individual Amplifiers $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		OP-227A OP-237A			OP-227C OP-237C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●	—	60	180	—	110	350	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●	—	0.2	1.0	—	0.3	1.8	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	—	15	50	—	30	135	nA
I_B	Input Bias Current		●	—	± 20	± 60	—	± 35	± 150	nA
	Input Voltage Range		●	± 10.5	± 11.8	—	± 10.2	± 11.8	—	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	108	122	—	94	116	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	—	2	16	—	4	51	$\mu V/V$
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	1	14	—	0.8	14	—	V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 11.5	± 13.5	—	± 10.5	± 13.0	—	V

The ● denotes the specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Note 2: Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs Time over extended periods after the first 30 days of operation.

Note 3: Sample tested.

Note 4: Parameter is guaranteed by design.

Note 5: See test circuit and frequency response curve for 0.1Hz to 10Hz tester.

Note 6: See test circuit for current noise measurement.

Note 7: The input offset drift performance is within the specifications un-nulled or when nulled with $R_p = 8k\Omega$ to $20k\Omega$.

Note 8: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds $\pm 0.7V$, the input current should be limited to 25mA.

Note 9: The V^+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V^- supply terminals are both connected to the common substrate and must be tied to the same voltage. Both V^- pins should be used.

MATCHING CHARACTERISTICS See notes on page 3.

at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	OP-227A, E, OP-237A, E			OP-227C, G, OP-237C, G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_{OS}	Input Offset Voltage Match		—	25	80	—	55	300	μV
I_B^+	Average Non-Inverting Bias Current		—	± 10	± 40	—	± 15	± 90	nA
I_{OS}^+	Non-Inverting Offset Current		—	± 12	± 60	—	± 20	± 130	nA
I_{OS}^-	Inverting Offset Current		—	± 12	± 60	—	± 20	± 130	nA
$\Delta CMRR$	Common Mode Rejection Ratio Match	$V_{CM} = \pm 11V$	110	123	—	97	117	—	dB
$\Delta PSRR$	Power Supply Rejection Ratio Match	$V_S = \pm 4V$ to $\pm 18V$	—	2	10	—	2	20	$\mu V/V$
	Channel Separation	(Note 4)	126	154	—	126	154	—	dB
ΔA_{VOL}	Gain Match	$f_0 = 100kHz$ (Note 4) $R_L \geq 2k\Omega$, $V_0 = \pm 10V$	—	1.5	6.0	—	2.0	9.0	%

at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted

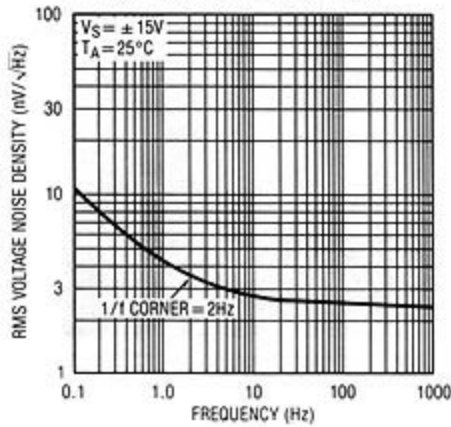
SYMBOL	PARAMETER	CONDITIONS	OP-227A, OP-237A			OP-227C, OP-237C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
ΔV_{OS}	Input Offset Voltage Match		●	—	55	180	—	100	480	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Tracking	(Note 7)	●	—	0.3	1.0	—	0.5	1.8	$\mu V/^\circ C$
I_B^+	Average Non-Inverting Bias Current		●	—	± 20	± 60	—	± 35	± 170	nA
$\frac{\Delta I_B^+}{\Delta Temp}$	Average Drift of Non-Inverting Bias Current		●	—	100	—	—	200	—	$pA/^\circ C$
I_{OS}^+	Non-Inverting Offset Current		●	—	± 25	± 90	—	± 45	± 250	nA
$\frac{I_{OS}^+}{\Delta Temp}$	Average Drift of Non-Inverting Offset Current		●	—	130	—	—	250	—	$pA/^\circ C$
I_{OS}^-	Inverting Offset Current		●	—	± 25	± 90	—	± 45	± 250	nA
$\Delta CMRR$	Common Mode Rejection Ratio Match	$V_{CM} = \pm 10V$	●	105	118	—	90	110	—	dB
$\Delta PSRR$	Power Supply Rejection Ratio Match	$V_S = \pm 4.5V$ to $\pm 18V$	●	—	2	16	—	4	51	$\mu V/V$

at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$, unless otherwise noted

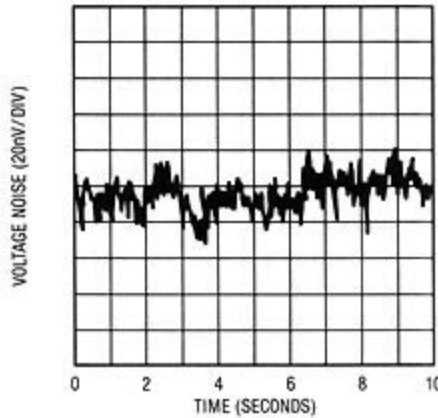
SYMBOL	PARAMETER	CONDITIONS	OP-227E, OP-237E			OP-227G, OP-237G			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
ΔV_{OS}	Input Offset Voltage Match		●	—	40	140	—	90	400	μV
$TC\Delta V_{OS}$	Input Offset Voltage Tracking	(Note 7)	●	—	0.3	1.0	—	0.5	1.8	$\mu V/^\circ C$
I_B^+	Average Non-Inverting Bias Current		●	—	± 14	± 60	—	± 25	± 170	nA
$\frac{\Delta I_B^+}{\Delta Temp}$	Average Drift of Non-Inverting Bias Current		●	—	80	—	—	180	—	$pA/^\circ C$
I_{OS}^+	Non-Inverting Offset Current		●	—	± 20	± 90	—	± 35	± 250	nA
$\frac{\Delta I_{OS}^+}{\Delta Temp}$	Average Drift of Non-Inverting Offset Current		●	—	130	—	—	250	—	$pA/^\circ C$
I_{OS}^-	Inverting Offset Current		●	—	± 20	± 90	—	± 35	± 250	nA
$\Delta CMRR$	Common Mode Rejection Ratio Match	$V_{CM} = \pm 10V$	●	106	120	—	90	112	—	dB
$\Delta PSRR$	Power Supply Rejection Ratio Match	$V_S = \pm 4.5V$ to $\pm 18V$	●	—	2	15	—	3	32	$\mu V/V$

TYPICAL PERFORMANCE CHARACTERISTICS

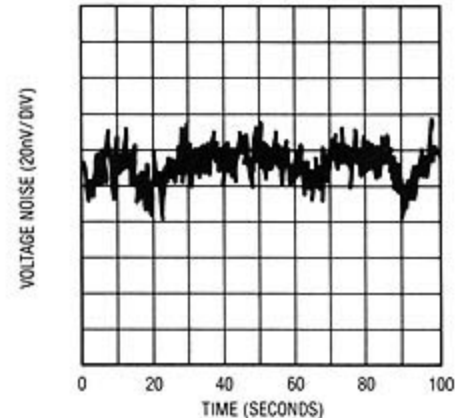
Voltage Noise vs Frequency



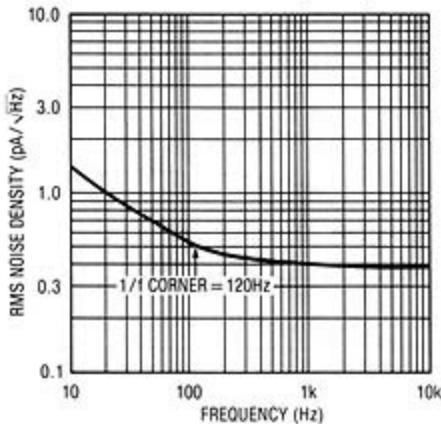
0.1Hz to 10Hz Noise



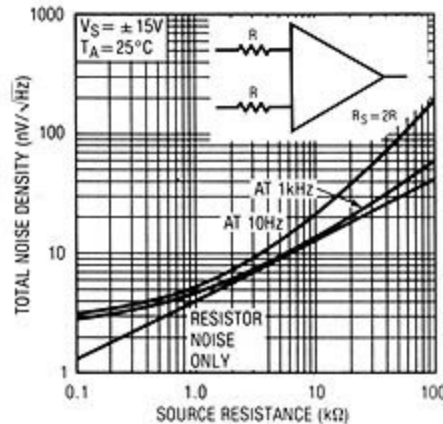
0.01Hz to 1Hz Peak-to-Peak Noise



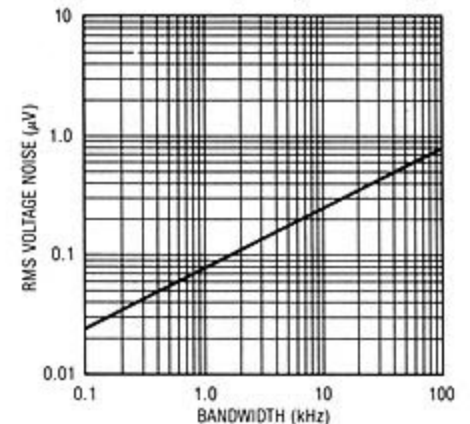
Current Noise vs Frequency



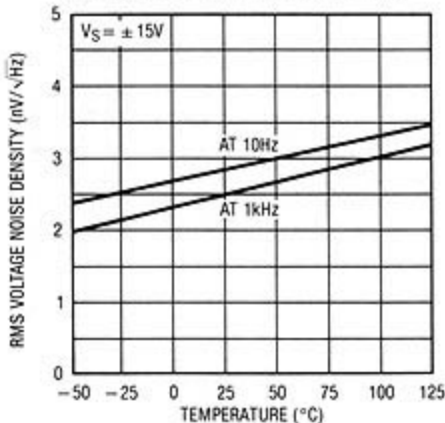
Total Noise vs Source Resistance



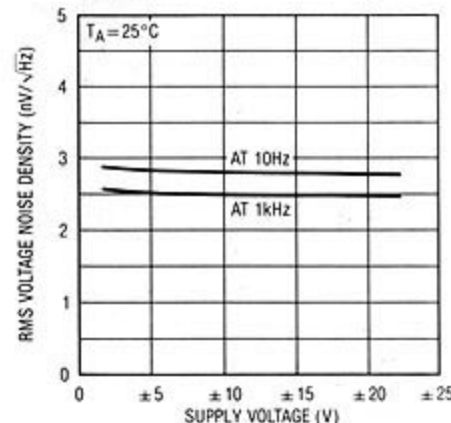
Wideband Voltage Noise (0.1Hz to Frequency Indicated)



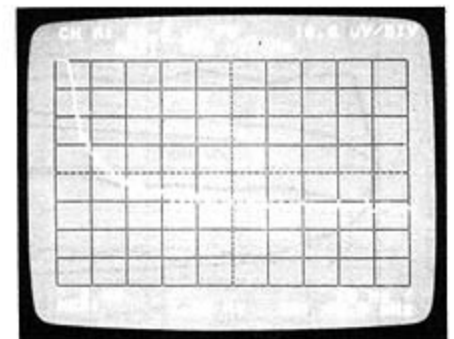
Voltage Noise vs Temperature



Voltage Noise vs Supply Voltage



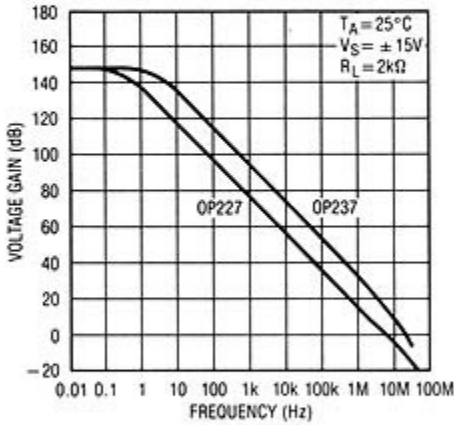
0.02Hz to 10Hz RMS Noise. Gain = 50,000 (Measured on HP3582 Spectrum Analyzer)



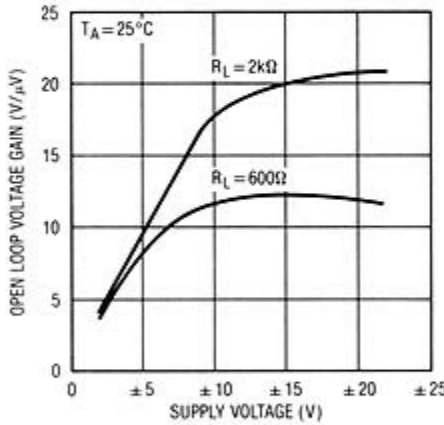
MARKER AT 2Hz (= 1/f CORNER) =
 $\frac{179 \mu\text{V}/\sqrt{\text{Hz}}}{50,000} = 3.59 \frac{\text{nV}}{\sqrt{\text{Hz}}}$

TYPICAL PERFORMANCE CHARACTERISTICS

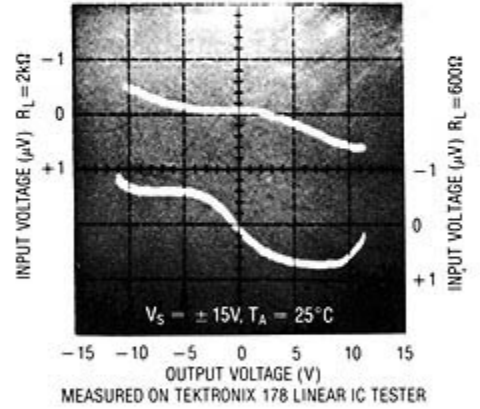
Voltage Gain vs Frequency



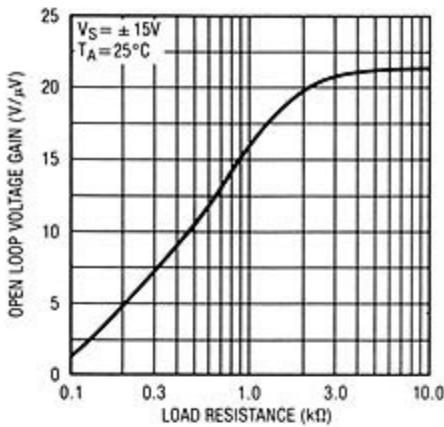
Voltage Gain vs Supply Voltage



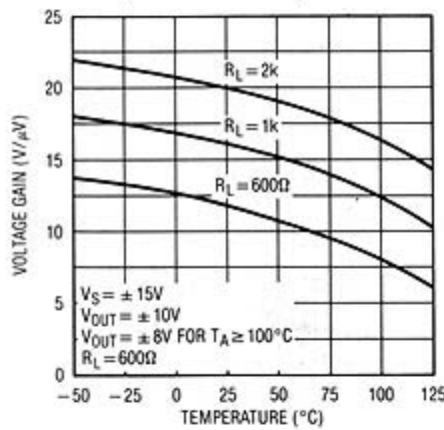
Voltage Gain, $R_L = 2k$ and 600Ω



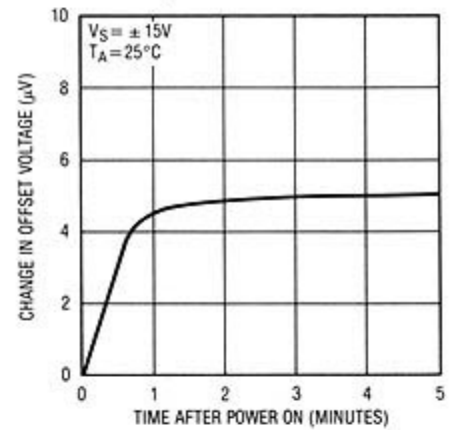
Voltage Gain vs Load Resistance



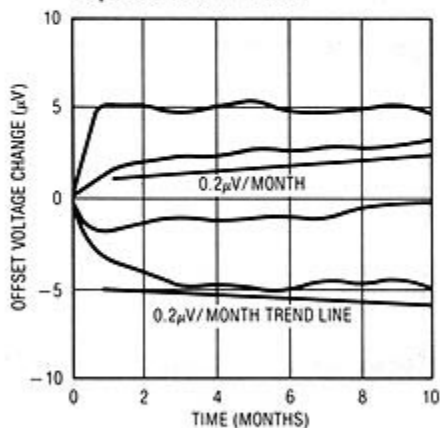
Voltage Gain vs Temperature



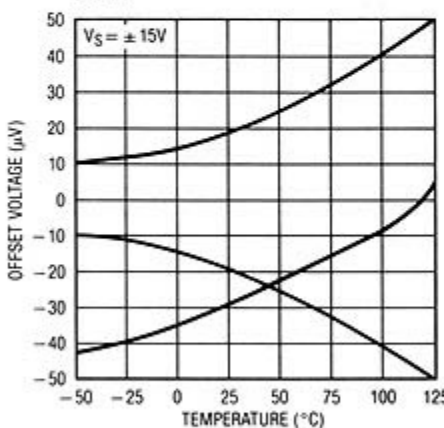
Warm-Up Drift



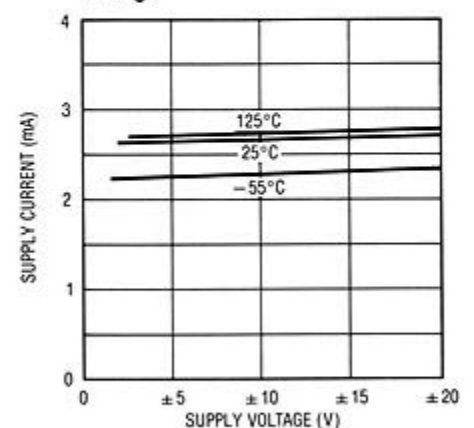
Long Term Stability of Four Representative Units



Offset Voltage Drift with Temperature of Representative Units

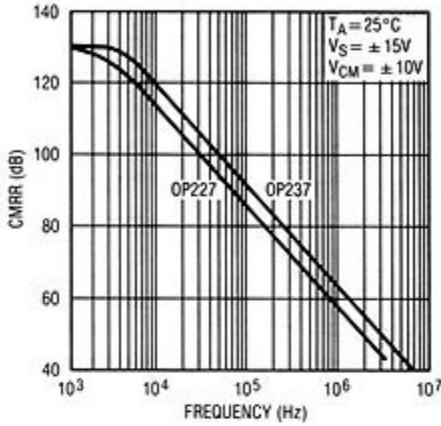


Supply Current vs Supply Voltage

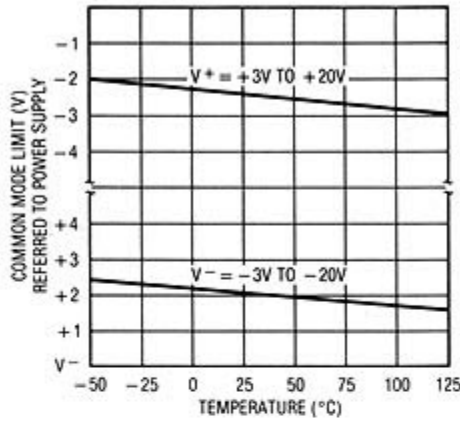


TYPICAL PERFORMANCE CHARACTERISTICS

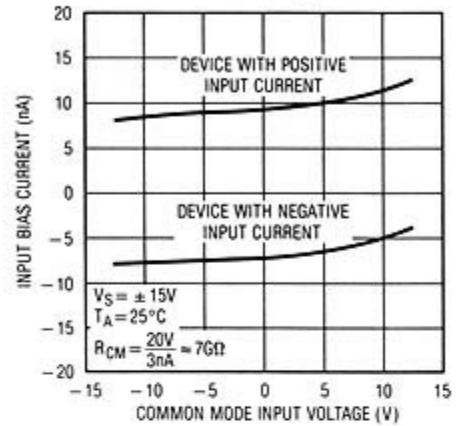
Common Mode Rejection vs Frequency



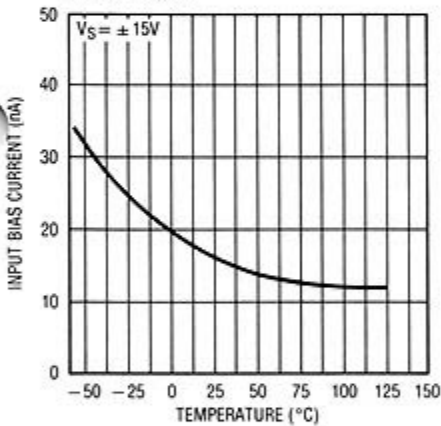
Common Mode Limit vs Temperature



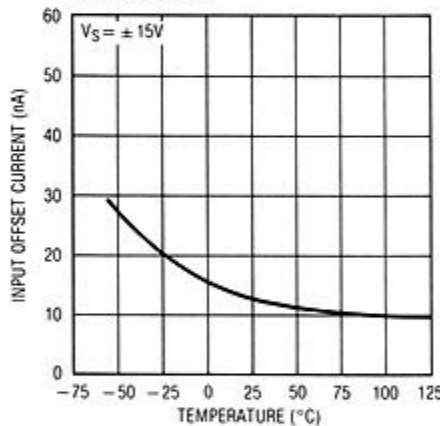
Input Bias Current Over the Common Mode Range



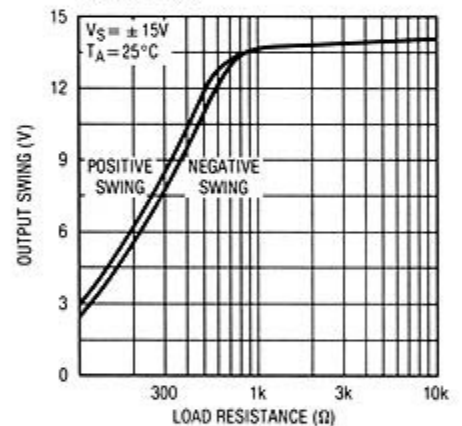
Input Bias Current vs Temperature



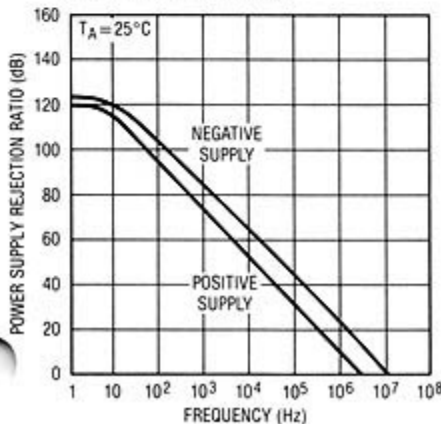
Input Offset Current vs Temperature



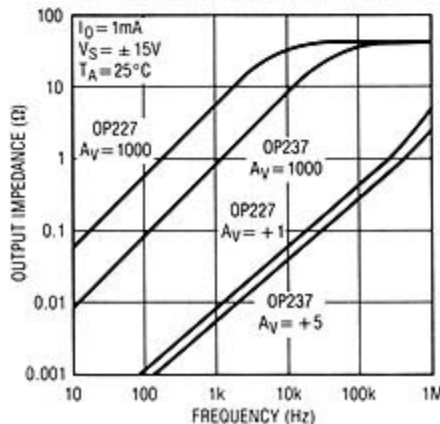
Output Swing vs Load Resistance



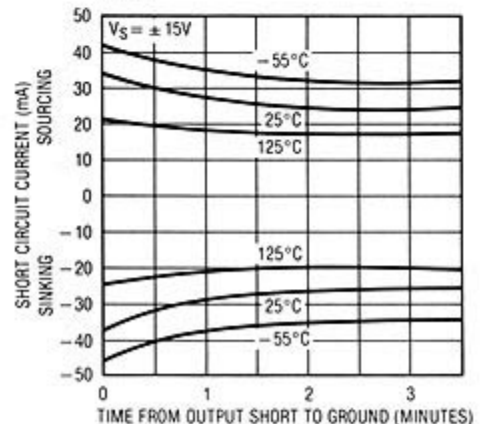
PSRR vs Frequency



Closed Loop Output Impedance

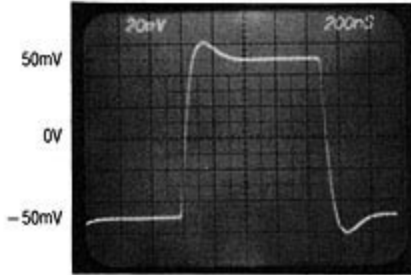


Output Short Circuit Current vs Time



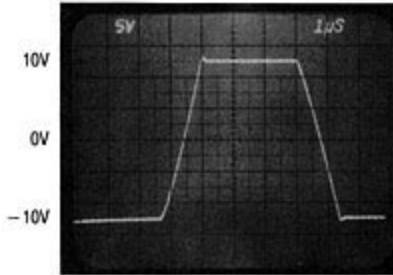
TYPICAL PERFORMANCE CHARACTERISTICS

OP-237 Small Signal Transient Response



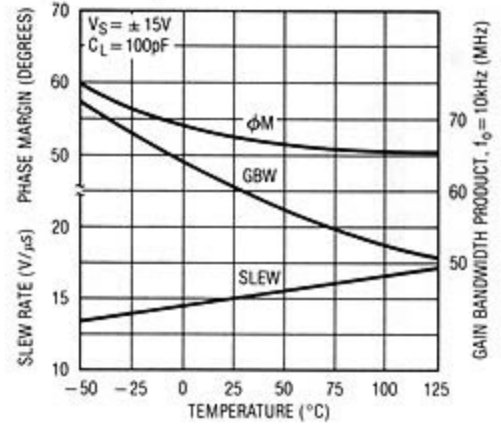
$A_{VCL} = +5, V_S = \pm 15V$
 $C_L = 15pF$

OP-237 Large Signal Response

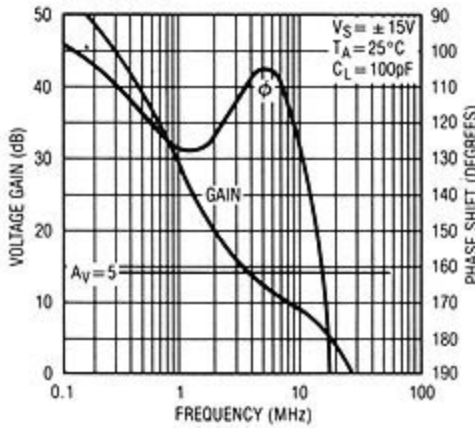


$A_{VCL} = +5, V_S = \pm 15V$

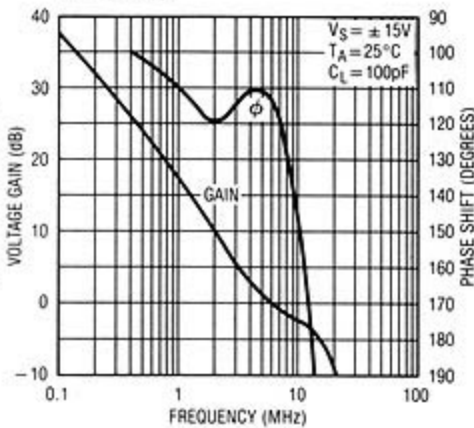
OP-237 Phase Margin, Gain Bandwidth Product, Slew Rate vs Temperature



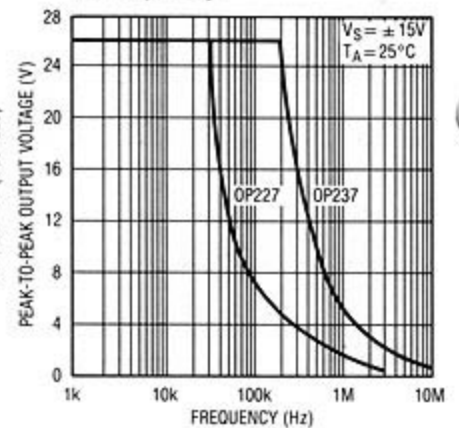
OP-237 Gain, Phase Shift vs Frequency



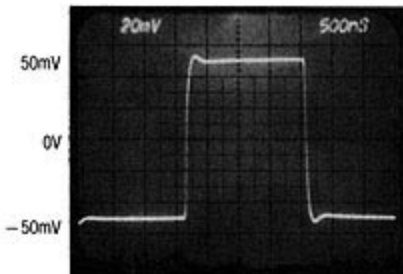
OP-227 Gain, Phase Shift vs Frequency



Maximum Undistorted Output vs Frequency

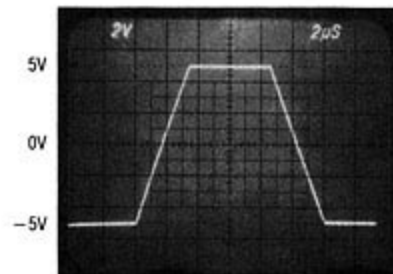


OP-227 Small Signal Transient Response



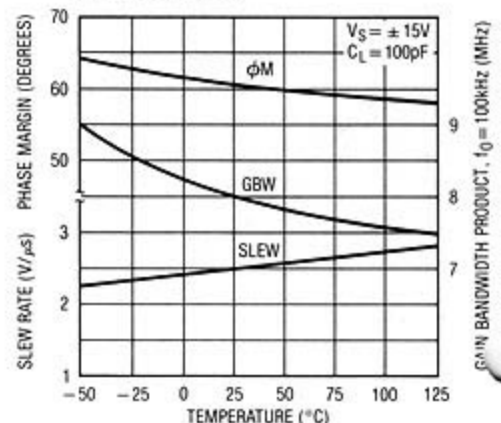
$A_{VCL} = +1, V_S = \pm 15V$
 $C_L = 15pF$

OP-227 Large Signal Response



$A_{VCL} = -1, V_S = \pm 15V$

OP-227 Phase Margin, Gain Bandwidth Product, Slew Rate vs Temperature



APPLICATIONS INFORMATION

Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the OP-227/OP-237 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

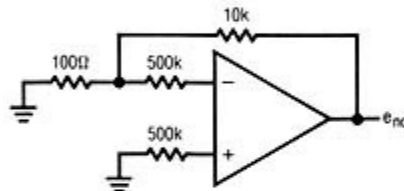
Measuring the typical 60nV peak-to-peak noise performance of the OP-227/OP-237 requires special test precautions:

- The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically $3\mu\text{V}$ due to its chip temperature increasing 10°C to 20°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.
- For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.
- Sudden motion in the vicinity of the device can also "feed through" to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the $1/f$ corner frequency.

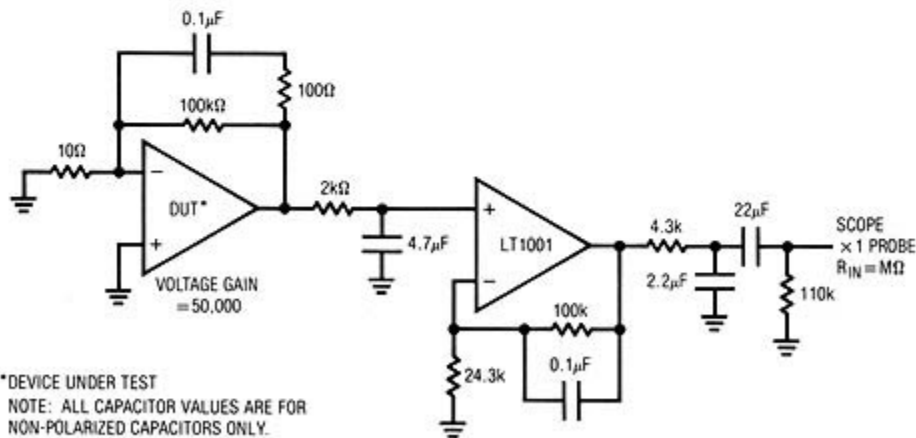
Current noise is measured in the circuit shown and calculated by the following formula:

$$i_n = \frac{[e^2_{no} - (130\text{nV})^2]^{1/2}}{1\text{M}\Omega \times 100}$$

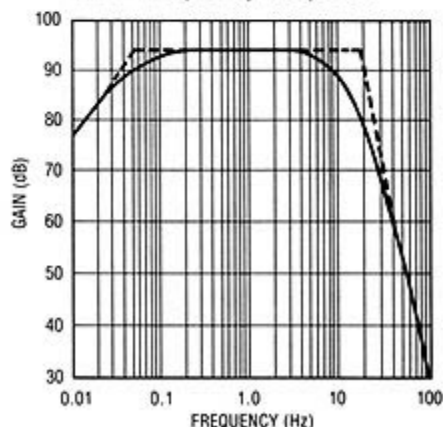


The OP-227/OP-237 achieves its low noise, in part, by operating the input stage at $120\mu\text{A}$ versus the typical $10\mu\text{A}$ of most other op amps. Voltage noise is inversely proportional, while current noise is directly proportional to the square root of the stage current. Therefore, the OP-227/OP-237 current noise will be relatively high. At low frequencies, the low $1/f$ current noise corner frequency ($\approx 120\text{Hz}$) minimizes current noise to some extent.

0.1Hz to 10Hz Noise Test Circuit



0.1Hz to 10Hz p-p Noise Tester Frequency Response



*DEVICE UNDER TEST
NOTE: ALL CAPACITOR VALUES ARE FOR
NON-POLARIZED CAPACITORS ONLY.

APPLICATIONS INFORMATION

In most practical applications, however, current noise will not limit system performance. This is illustrated in the total noise versus source resistance plot, where total noise = $[(\text{voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise})^2]^{1/2}$.

Three regions can be identified as a function of source resistance:

- (i) $R_S \leq 400\Omega$ - Voltage noise dominates

- (ii) $400\Omega \leq R_S \leq 50k\Omega$ at 1kHz Resistor noise dominates
 $400\Omega \leq R_S \leq 8k\Omega$ at 10Hz
- (iii) $R_S > 50k\Omega$ at 1kHz Current noise dominates
 $R_S > 8k\Omega$ at 10Hz

Clearly the OP-227/OP-237 should not be used in region (iii), where total system noise is at least six times higher than the voltage noise of the op amp, i.e., the low voltage noise specification is completely wasted.

APPLICATIONS INFORMATION

OP AMP MATCHING

Advantages of Matched Dual Op Amps

In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

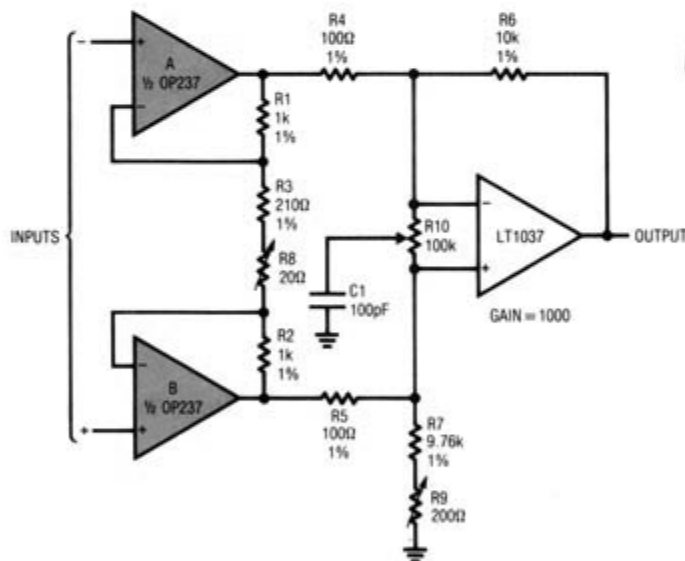
The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the OP-227/OP-237. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two non-inverting input currents (I_B^+). The difference between these two currents (I_{OS}^+) is the offset current of the instrumentation amplifier. The difference between the inverting input currents (I_{OS}^-) will cause errors flowing through R1, R2, and R3. Common mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

The concepts of common mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

Assume $\text{CMRR}_A = +1.0\mu\text{V}/\text{V}$ or 120dB,
 and $\text{CMRR}_B = +0.75\mu\text{V}/\text{V}$ or 122.5dB,
 then $\Delta\text{CMRR} = 0.25\mu\text{V}/\text{V}$ or 132dB;
 if $\text{CMRR}_B = -0.75\mu\text{V}/\text{V}$ which is still 122.5dB,
 then $\Delta\text{CMRR} = 1.75\mu\text{V}/\text{V}$ or 115dB.

Clearly, the OP-227/OP-237, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching dependent circuits.

Three Op Amp Instrumentation Amplifier



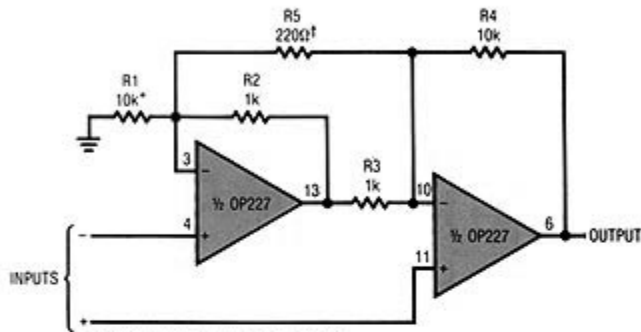
- Trim R8 for gain
- Trim R9 for DC common mode rejection
- Trim R10 for AC common mode rejection

Typical performance of the instrumentation amplifier:

- Input offset voltage = $60\mu\text{V}$
- Input bias current = $\pm 15\text{nA}$
- Input offset current = $\pm 20\text{nA}$
- Input noise = $0.08\mu\text{Vp-p}$
- Power bandwidth ($V_O = \pm 10\text{V}$) = 250kHz

APPLICATIONS INFORMATION

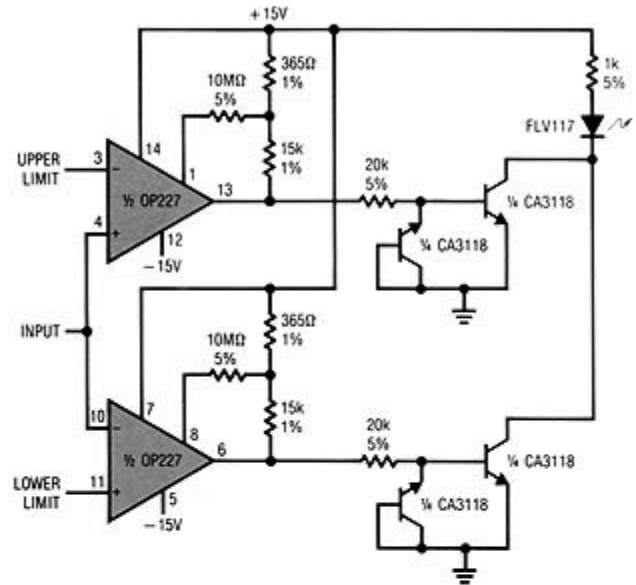
Two Op Amp Instrumentation Amplifier



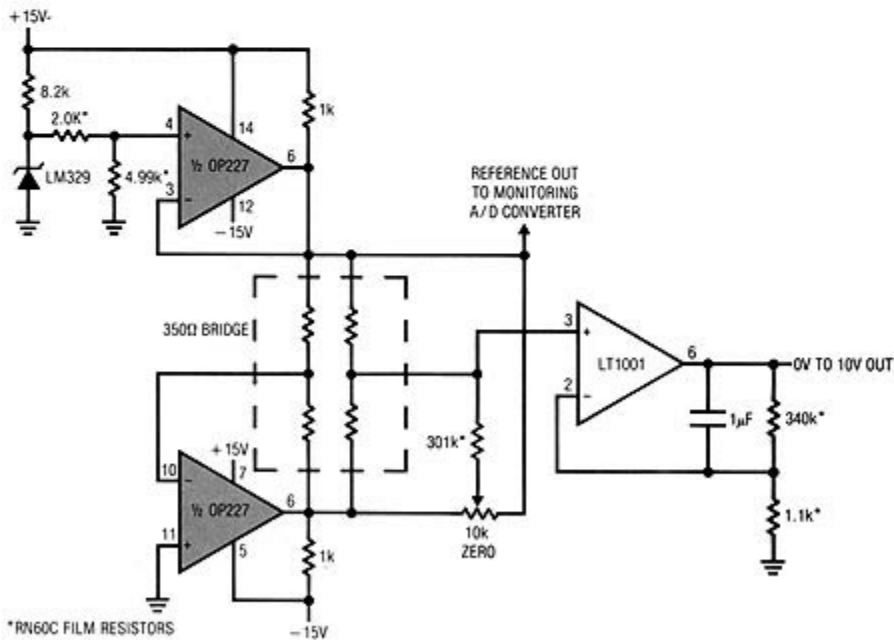
*TRIM FOR COMMON MODE REJECTION
†TRIM FOR GAIN

$$GAIN = \frac{R4}{R3} \left[1 + \frac{1}{2} \left(\frac{R2}{R1} + \frac{R3}{R4} \right) + \frac{R2+R3}{R5} \right] = 100$$

Dual Limit Microvolt Comparator

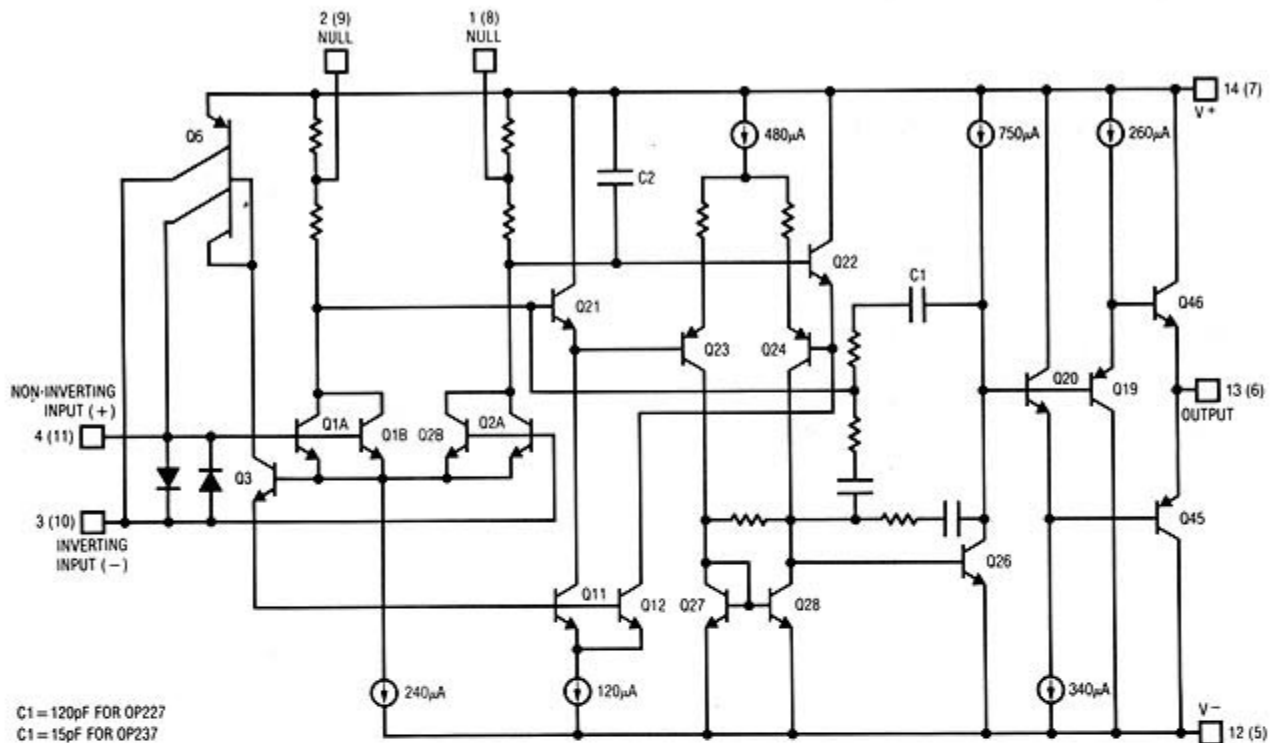


Strain Gauge Signal Conditioner with Bridge Excitation



*RN60C FILM RESISTORS

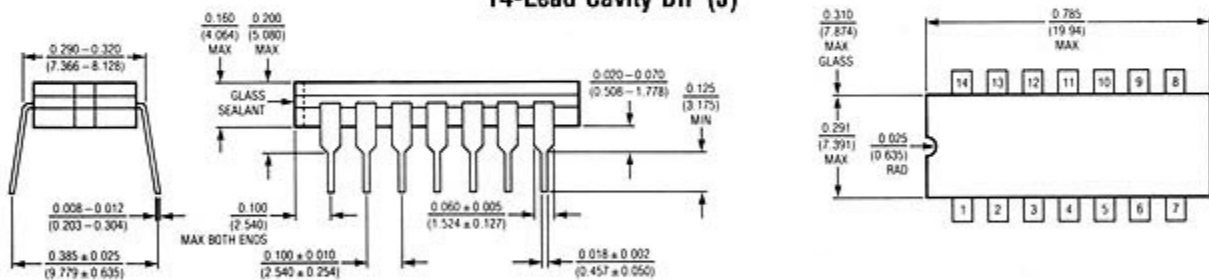
SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

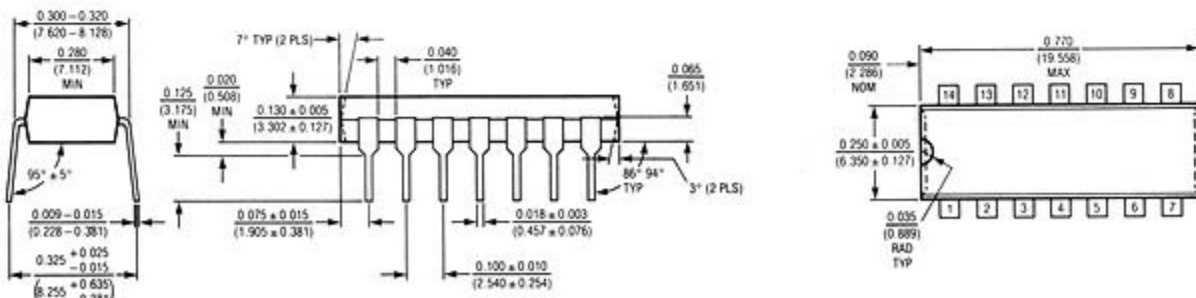
Dimensions in inches (millimeters) unless otherwise noted.

14-Lead Cavity DIP (J)



OP-227EJ	OP-237EJ	T_{JMAX}	θ_{JA}
OP-227GJ	OP-237GJ	125°C	100°C/W
OP-227AJ	OP-237AJ	150°C	100°C/W
OP-227CJ	OP-237CJ		

14-Lead Molded DIP (N)



OP-227EN	OP-237EN	T_{JMAX}	θ_{JA}
OP-227GN	OP-237GN	125°C	100°C/W